# Homework 2

(Due date: September 26th)

Presentation and clarity are very important! Show your procedure!

## PROBLEM 1 (36 PTS)

- Calculate the result (provide the 32-bit result) of the following operations with 32-bit floating point numbers. Truncate the results when required. When doing fixed-point division, use 8 fractional bits. Show your procedure.

| | | | |
|---|---|---|---|
| ✓ 3DE38C80 + 3A80D980 | ✓ 80A18000 – 03CEC000 | ✓ 7A09C000 × 8BEE0000 | ✓ 7A390000 ÷ C8400000 |
| ✓ 80123000 + 804E8000 | ✓ 09DECAF0 – 7AD90000 | ✓ FA19D800 × CD100000 | ✓ 7F800000 ÷ CAB34C00 |
| ✓ 7FBEADED + FACADE90 | ✓ F0B1ABEE – 7F800000 | ✓ 0B094000 × 8FBEE000 | ✓ C9680000 ÷ 80700000 |

## PROBLEM 2 (8 PTS)

- Complete the table for the following DFX formats:

| DFX format | $p_0$ | $p_1$ | Number of bits of significand | Boundary value | $num0$ range | $num1$ range | Dynamic Range (dB) |
|---|---|---|---|---|---|---|---|
| 8_4_2 | | | | | | | |
| 12_7_5 | | | | | | | |
| 16_8_3 | | | | | | | |
| 24_15_9 | | | | | | | |

## PROBLEM 3 (16 PTS)

- Convert the following signed fixed-point numbers in format [16 8] to the dual fixed point format 16_8_3. If more bits are required, you are allowed to use the format 17_8_3.

| FX | FA.1C | 0A.B7 | 89.7C | 9C.1F | 83.FE | 7E.25 | B1.4B | 6D.E9 |
|---|---|---|---|---|---|---|---|---|
| DFX | | | | | | | | |

## PROBLEM 4 (30 PTS)

- Calculate the result of the following operations where the numbers are represented in dual fixed-point arithmetic. Note that the results must be in the same format. Include an overflow bit when necessary.

| **DFX Format: 8_4_2** | Result | overflow | | Result | overflow |
|---|---|---|---|---|---|
| FA+0B | | | F9-90 | | |
| 79+43 | | | A2+EC | | |
| C4+C3 | | | 34+FC | | |

| **DFX Format 16_8_4** | Result | overflow | | Result | overflow |
|---|---|---|---|---|---|
| FA2A+0A0E | | | C010+F2C4 | | |
| A004+B1C3 | | | F93A-0932 | | |
| 6A9A-F34C | | | 207F-31DE | | |

# PROBLEM 5 (10 PTS)

- Complete the timing diagram of the following iterative unsigned multiplier ($N = 4, M = 4$).
  Register: $sclr$: synchronous clear. Here, if $sclr = E = 1$, the register contents are initialized to 0.
  Parallel access shift register: If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift